BEE 332 Devices and Circuits II
Spring 2017
Lab 3: Multi-transistor circuits instructor's notes*

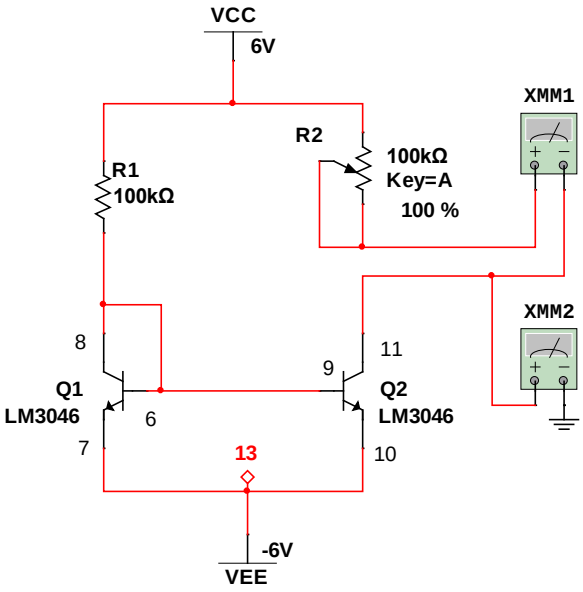
3 Current mirror

3.1 Circuit

You were asked to build this circuit. Meter 1 measures IC2, meter 2 measures VC2.

My measured values:

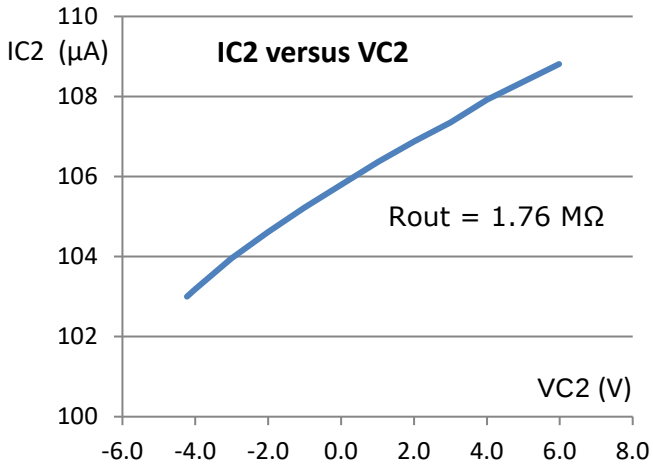
VCC = 5.98 V
VEE = -5.98 V
R1 = 99.39 KΩ



3.2 Measurements

You were asked to adjust R2 to vary the collector voltage of Q2 from 6.0 V to about –5.0 V to simulate different current loads. It's pretty flat. My results:

VC2 (V)	IC2 (µA)
5.980	108.81
4.000	107.92
2.998	107.35
2.012	106.88
1.015	106.37
0.024	105.81
-1.015	105.22
-2.009	104.61
-3.012	103.95
-4.010	103.18
-4.230	103.00



* These notes were written by Nicole Hamilton.

3.3 Analysis

1. Calculate IC1 assuming β = 110.

The old instructions didn't ask that you measure VB1, so I didn't. But let's suppose VBE1 ≈ 0.7 V and assume IB1 = IB2 because they're matched.

$$I_{R1} = \frac{V_{CC} - V_{EE} - V_{BE1}}{R1} = 113\ \mu A$$

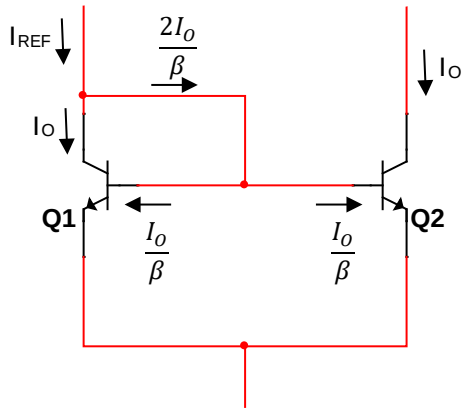
$$I_{R1} = I_{C1} + 2\ I_{B1}$$

$$I_{B1} = \frac{I_{C1}}{\beta}$$

$$I_{R1} = I_{C1} + 2\ \frac{I_{C1}}{\beta}$$

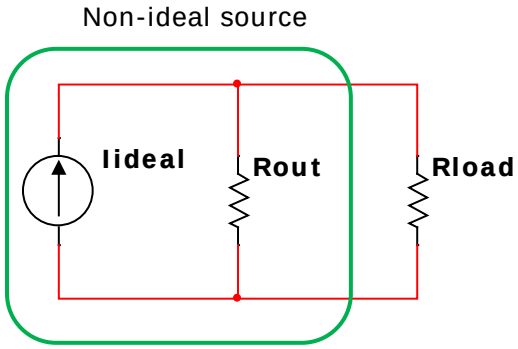
$$I_{R1} = I_{C1}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C1} = \frac{I_{R1}}{1 + \frac{2}{\beta}} = 111\ \mu A$$



2. Plot IC2 versus VC2 on the X-axis. (Above.)
3. Calculate Rout = ΔV / ΔI. (By KCL, any ΔI must be going into Rout.)

   Rout = (5.98 + 4.23) V / (108.81 – 103.00) μA
   = 1.76 MΩ



4. Explain the purpose of connection between the base and collector of Q1.

   It establishes that Q1 and Q2 will both be operating in forward active mode and that the base, and thus the collector currents will be matched.

5. Explain why VC2 can't be brought all the way down to VEE = -6.0 V.

   There's a diode drop across Q2. Also, some of you may have circuits like mine, where the mirror is fixed to create a current of about 105 μA. Maximum resistance of the pot R2 is 100 KΩ, meaning VR2 max is 105e-6 * 100e3 = 10.3 V. This is less than the VCC – VEE = 12 V. Minimum VC should be about -6 + (12 – 10.3) = –4.3 V, roughly as measured.

6. Explain if and how the current source is sensitive to the values of the PS voltages.

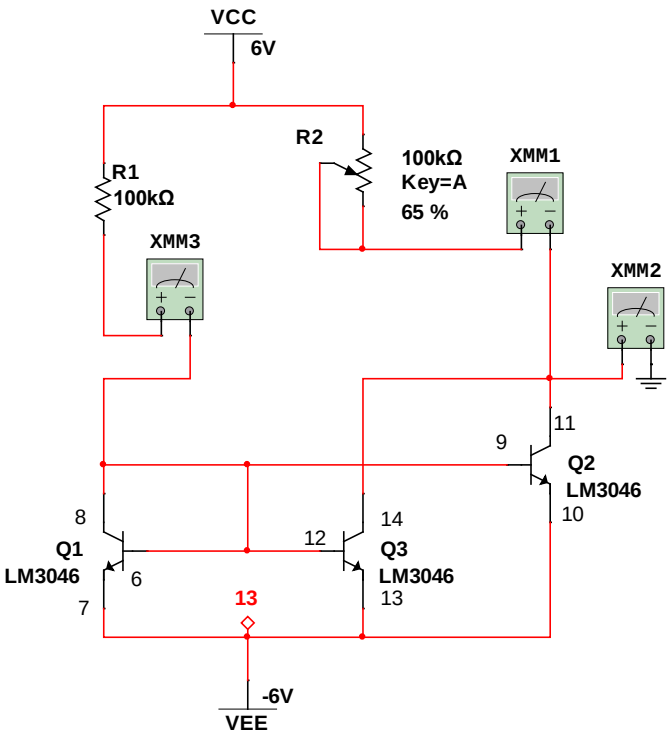
   It will be linear with the PS voltages because the current through Q1 is set as follows and will be mirrored in Q2 assuming it also is kept in forward active mode. From above,

$$I_{R1} = \frac{V_{CC} - V_{EE} - V_{BE1}}{R1}$$

$$I_{C1} = \frac{I_{R1}}{1 + \frac{2}{\beta}} = \frac{\left(\frac{V_{CC} - V_{EE} - V_{BE1}}{R1}\right)}{1 + \frac{2}{\beta}} = \frac{V_{CC} - V_{EE} - V_{BE1}}{R1\left(1 + \frac{2}{\beta}\right)}$$

7. Design a current source for which the output current is exactly twice that of the reference current using 3 BJTs from the CA3046 array.

   The expected design would put two transistors in parallel in the output as shown here.



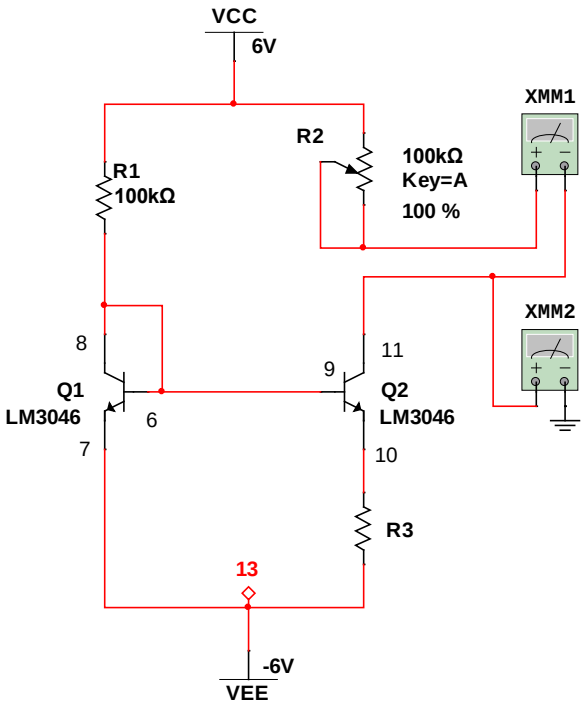
4 Widlar reducing current source

4.1 Circuit

You were asked to add R3 to the Q2 emitter circuit.

The value of R3 was to be set to produce IC2 = 10 µA according to the formula:

$$R_3 = \frac{V_T ln\left(\frac{I_{C1}}{I_{C2}}\right)}{I_{C2}}$$



1. Derive this equation starting from

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

As follows:

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$V_{BE} = V_T ln\left(\frac{I_C}{I_S}\right)$$

$$V_{B1} = V_{EE} + V_{BE1}$$

$$V_{B2} = V_{EE} + I_{E2}R_3 + V_{BE2}$$

$$V_{B1} = V_{B2}$$

$$V_{EE} + V_{BE1} = V_{EE} + I_{E2}R_3 + V_{BE2}$$

$$V_{BE1} = I_{E2}R_3 + V_{BE2}$$

$$I_{E2} \cong I_{C2}$$

$$V_T ln\left(\frac{I_{C1}}{I_S}\right) = I_{C2}R_3 + V_T ln\left(\frac{I_{C2}}{I_S}\right)$$

$$V_T\left[ln\left(\frac{I_{C1}}{I_S}\right) - ln\left(\frac{I_{C2}}{I_S}\right)\right] = I_{C2}R_3$$

$$V_T ln\left(\frac{\frac{I_{C1}}{I_S}}{\frac{I_{C2}}{I_S}}\right) = I_{C2}R_3$$

$$V_T ln\left(\frac{I_{C1}}{I_{C2}}\right) = I_{C2}R_3$$

$$R_3 = \frac{V_T ln\left(\frac{I_{C1}}{I_{C2}}\right)}{I_{C2}}$$

2. Calculate the value of R3 for this Widlar current source to produce IC2 = 10 μA. You may assume IC1 is the same as you measured in the previous procedure.

   From procedure 1, IC1 ≈ 111 μA, so R3 should be ≈ 6.017 KΩ.

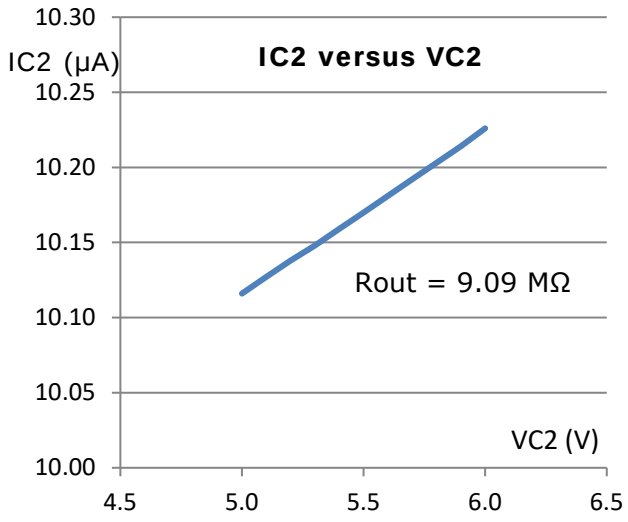
   I used 6.8 KΩ.

3. Measured values:

   R1 = 99.39 KΩ
   R3 = 6.68 KΩ
   VCC = 6.0133 V
   VEE = -6.0133 V

4.2 Measurements

VC2 (V)	IC2 (μA)	VB1 = VC1
5.000	10.116	-5.350
5.100	10.127	-5.350
5.200	10.138	-5.350
5.300	10.148	-5.350
5.400	10.159	-5.350
5.500	10.170	-5.350
5.600	10.181	-5.350
5.700	10.192	-5.350
5.900	10.214	-5.350
6.000	10.226	-5.350



4.3 Analysis

1. Plot IC2 versus VC2. (Above.)
2. Calculate the output resistance.

   Rout = ΔV / ΔI = (6.0 – 5.0) V / (10.226 / 10.116) μA = 9.09 MΩ

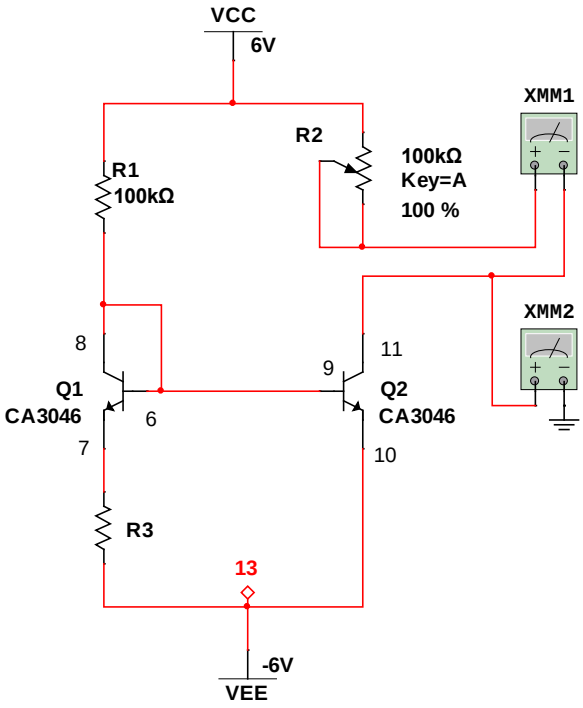
5 Widlar boosting source

5.1 Circuit

You were asked to move R3 to the emitter of Q1 and again measure IC2 versus VC2.

The value of R3 was to be set to produce IC2 = 1 mA according to the formula:

$$R_3 = \frac{V_T ln\left(\frac{I_{C2}}{I_{C1}}\right)}{I_{C1}}$$



1. Calculate the value of R3.

   I assumed IC1 ≈ 111 μA, so R3 should be about 495 Ω.

   I used 470 Ω.

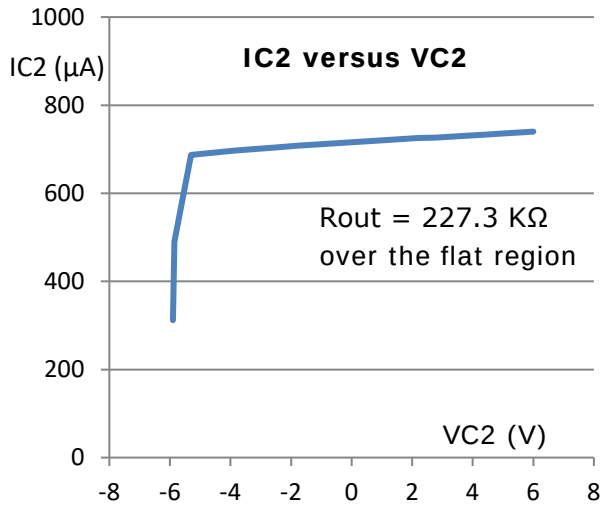
2. Measured values:

   R1 = 99.39 KΩ
   R3 = 469 Ω
   VCC = 6.0133 V
   VEE = -6.0133 V

5.2 Measurements

These were my results, likely typical. You don't need this many data points to get credit.

VC2 (V)	IC2 (µA)	VB1 = VC1
6.000	740.000	-5.320
5.530	737.80	-5.320
5.170	736.40	-5.320
4.510	733.74	-5.320
3.810	731.00	-5.320
2.775	726.33	-5.320
2.225	725.44	-5.320
1.564	722.72	-5.320
-0.088	715.48	-5.320
-1.761	707.96	-5.320
-2.546	704.06	-5.320
-3.670	697.90	-5.320
-4.040	695.82	-5.320
-5.300	687.04	-5.320
-5.850	490.42	-5.320
-5.900	311.94	-5.330



5.3 Analysis

1. Plot IC2 versus VC2. (Above.)
2. Calculate the output resistance of the boosting Widlar current source.

   Over the flat range down to -4.04 V.

   Rout = ΔV / ΔI = (6.0 +4.04) V / (740.0 – 695.82) µA = 227.3 KΩ

3. Explain why the output resistance of the reducing source is higher than the boosting case.

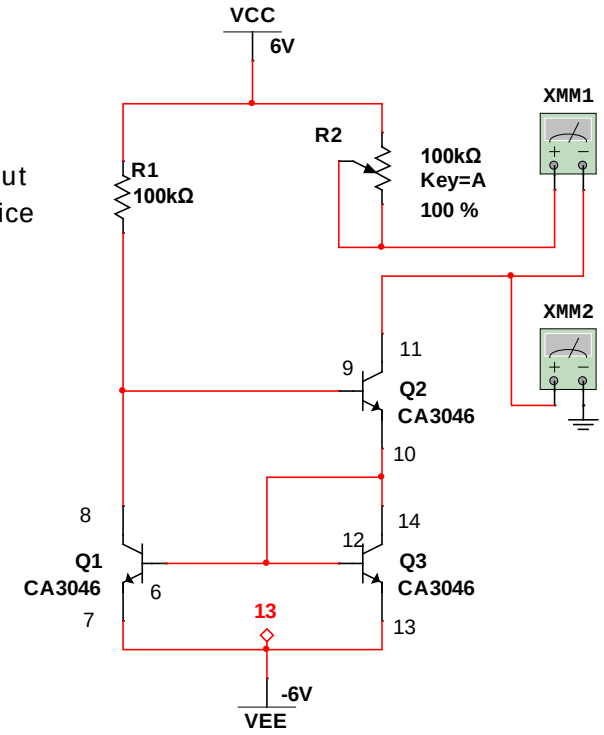
   In the reducing source, R3 is in the emitter circuit of Q2. If IE2 were to increase (or fall), the IR drop across R3 would increase (fall), causing VBE2 to fall (rise), in turn causing IC2 (and thus IE2) to fall (rise).

   The result is a negative feedback loop. If IE changes, Q2 will invert and amplify the effect of any voltage change across R3, restoring IE. This has the effect of multiplying the effect of R3 and making this a more ideal current source, albeit one that only produces a much smaller current.

6 Wilson current source

6.1 Circuit

You were asked to build this circuit to increase output resistance and again measure IC2 versus VC2. Notice the much flatter curve for IC2.



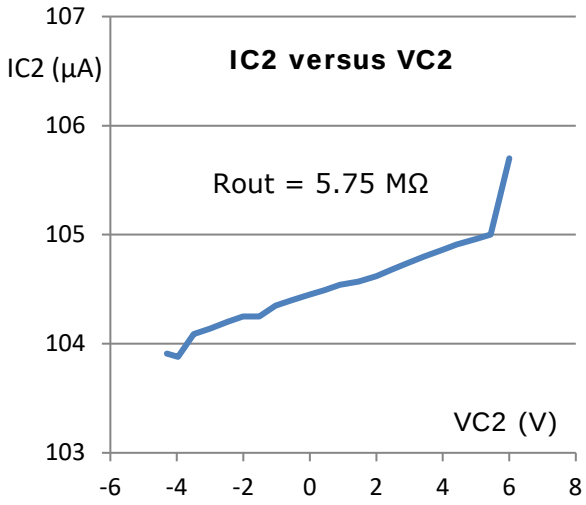
Measured values:

R1 = 99.39 KΩ
VCC = 6.0059 V
VEE = -6.0059 V

Measurements

6.2

VC2 (V)	IC2 (µA)	VB1	VC1
6.00	105.70	-4.55	-4.03
5.44	105.00	-4.52	-4.01
5.00	104.96	-4.52	-4.03
4.42	104.91	-4.53	-4.00
3.99	104.86	-4.52	-4.03
3.43	104.80	-4.52	-4.03
2.95	104.74	-4.52	-4.02
2.47	104.68	-4.52	-4.02
2.00	104.62	-4.51	-3.99
1.46	104.57	-4.51	-4.02
0.91	104.54	-4.52	-4.02
0.44	104.49	4.52	-4.01
-0.02	104.45	-4.50	-4.04
-0.54	104.40	-4.51	-4.03
-1.03	104.35	-4.51	-4.03
-1.52	104.25	-4.50	-3.92
-2.01	104.25	-4.50	-3.87
-2.48	104.20	-4.51	-3.45
-3.00	104.14	-4.51	-4.01
-3.49	104.09	-4.51	-4.01
-3.960	103.88	-4.5	-3.02
-4.300	103.91	-4.5	-2.91



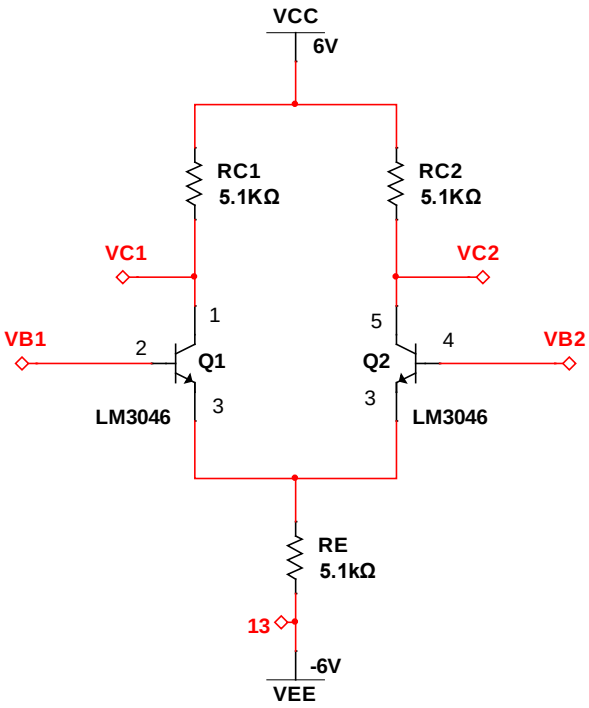
6.3 Analysis

1. Plot IC2 versus VC2. (Above.)
2. Calculate the output resistance of the Wilson current source.

   Rout = ΔV / ΔI = (6 + 4.3) V / (105.7 – 103.91) μA = 5.75 MΩ

7 Differential amplifier

You were asked to build this circuit.



Measured values:

RC1 = 5.04 KΩ
RC2 = 5.04 KΩ
RE = 5.03 KΩ
VCC = 6.0097 V
VEE = -6.0097 V

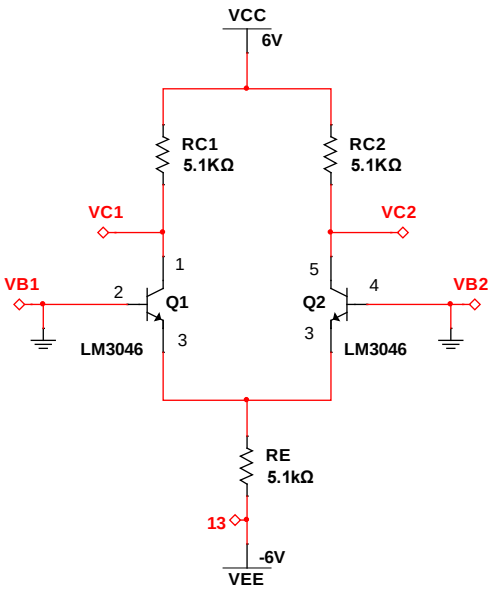
7.1 Grounded inputs

With both VB1 and VB2 grounded:

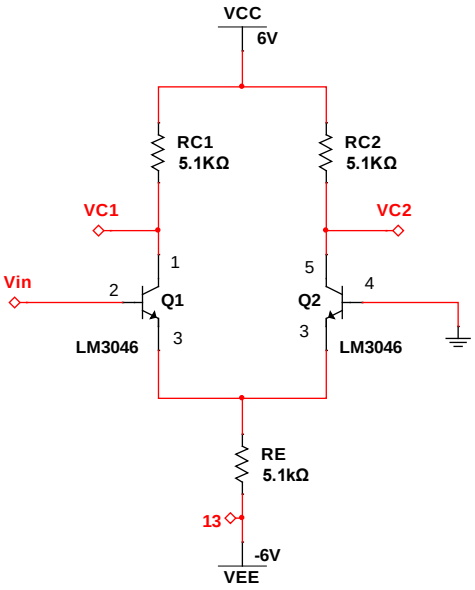
VC1 = VC2 = 3.363 V
VB1 = VB2 = 0
VE1 = VE2 = -0.70635 V

7.2 Differential mode

You were then asked to reconfigure the circuit with Vin applied to VB1 and VB2 grounded.

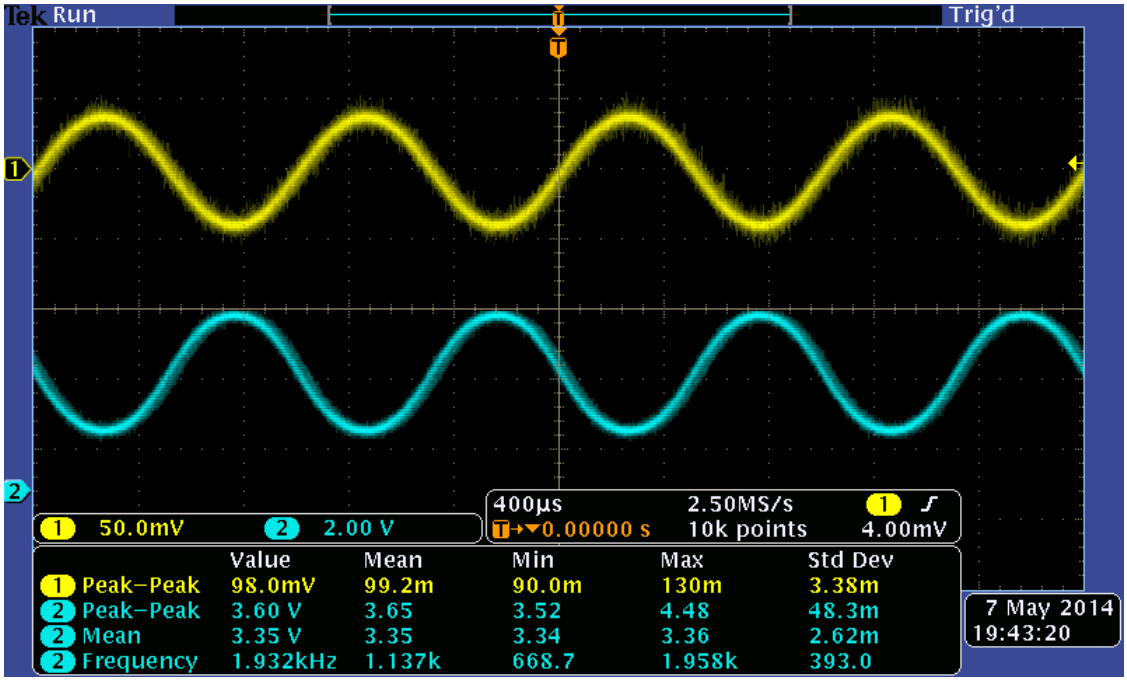


Grounded inputs.

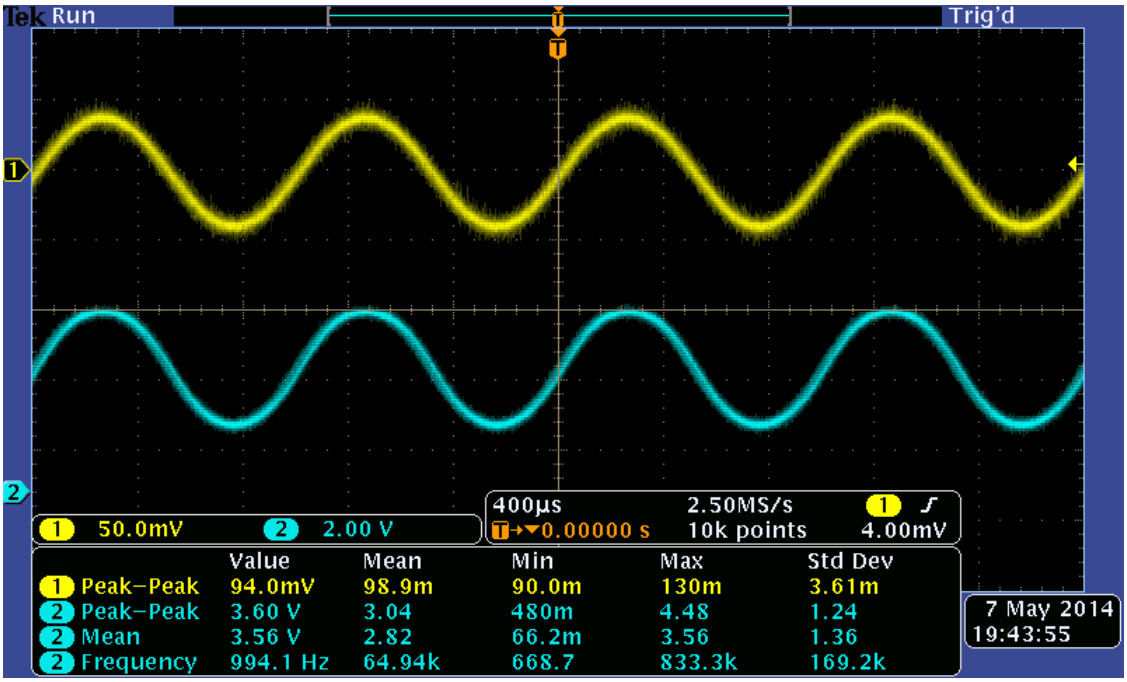


Differential mode.

1. With Vin = 100 mVpp, 1 KHz sine wave, this was VC1 versus Vin. Notice that VC1 is inverting and VC2 is not. Each side looks like a CE amplifier, where gain would be RC/RE. Here, it's much higher. IRE in a CE amplifier = (β + 1)*IRC, causing VE to rise, creating negative feedback. But with the differential pair, the other transistor compensates. As the current through Q1 rises, it falls in Q2.

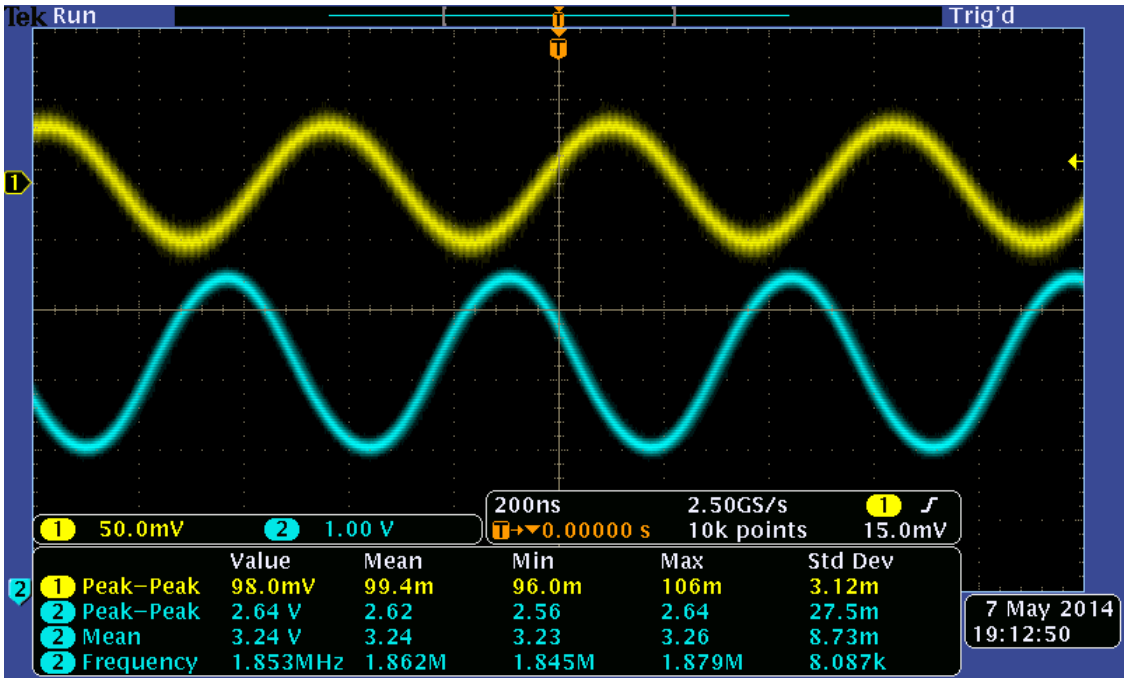


And this was VC2 versus Vin.



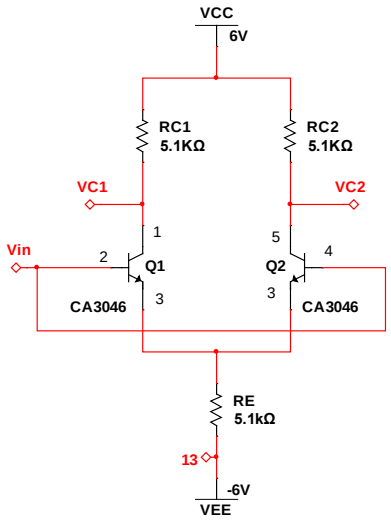
2. Av1 = VC1/Vin = –3.60/.098 = -36.7
   Av2 = VC2/Vin = 3.60/.094 = 38.3.

3. The 3 db point is where Av drops to .7071 * 37.3 = 26.4. This shows Av = 2.62 V / 99.4 mV = 26.4 at 1.86 MHz. (I wasn't clear in the instructions; you only needed to find the 3 dB point for either Av1 or Av2, not both.)

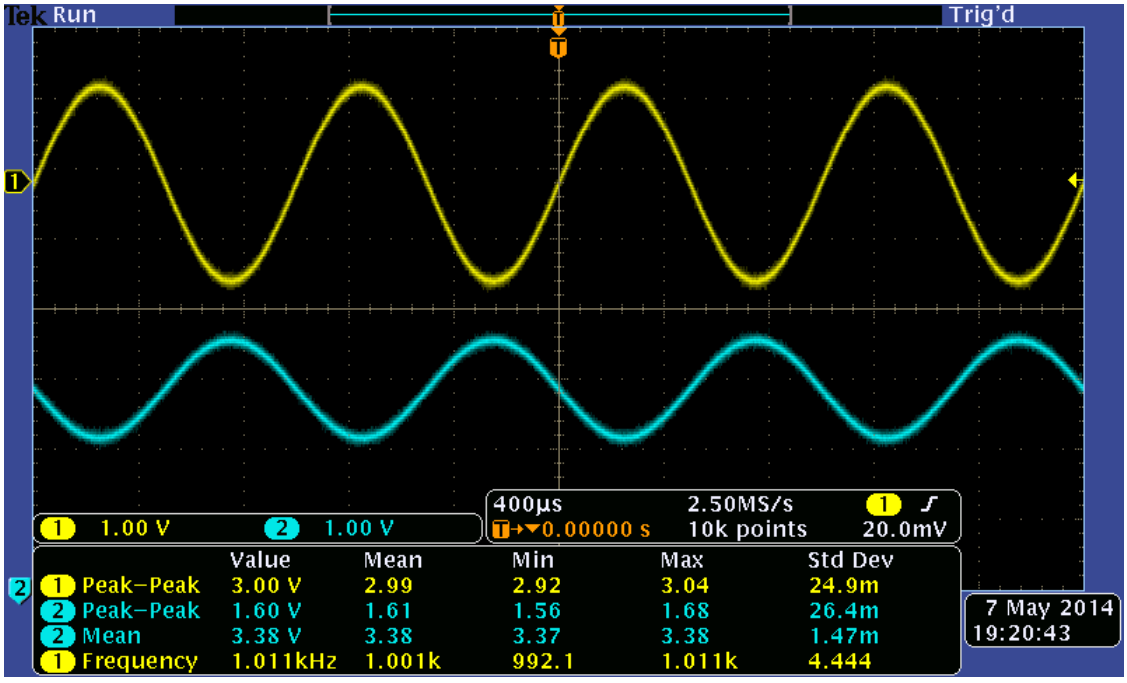


7.3 Common mode

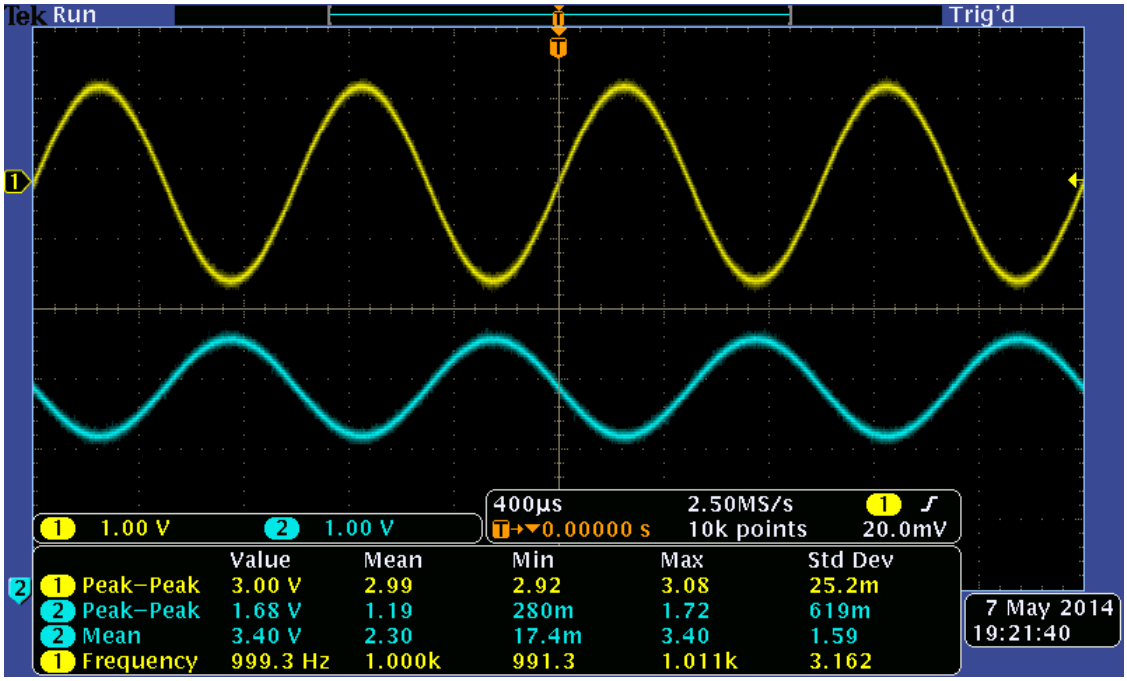
Next, you were asked to modify the circuit to apply Vin to both VB1 and VB2 to measure common mode gain.



1. You were asked to measure with Vin = 3 Vpp, 1 KHz sine wave.
   This shows VC1.

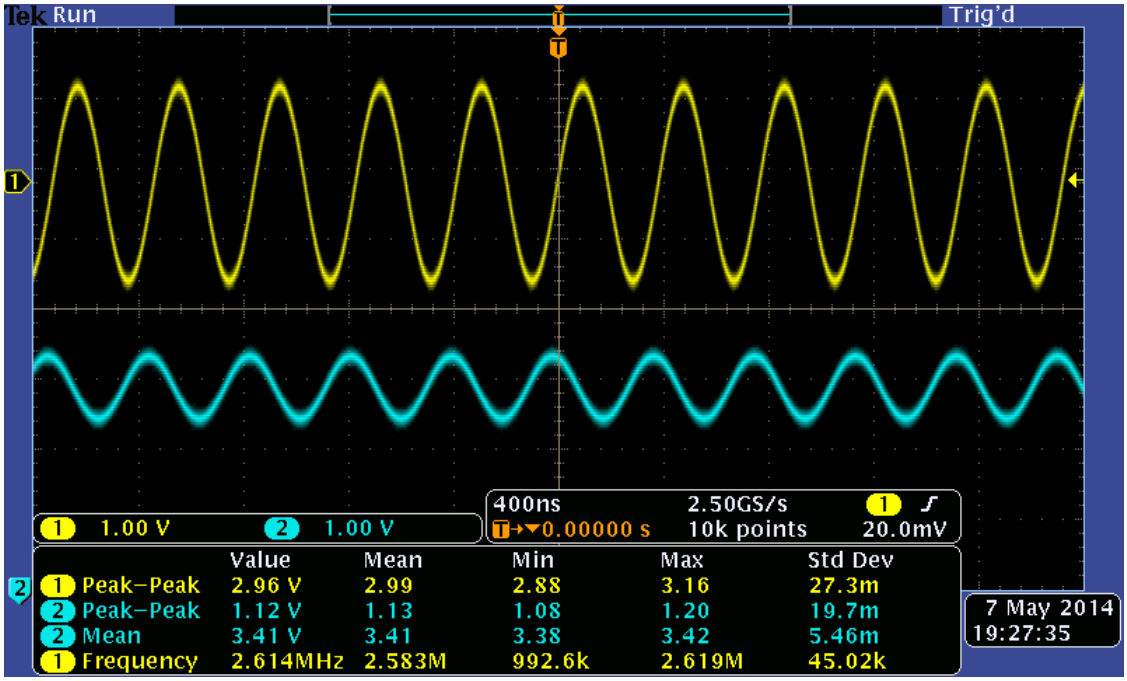


And here is VC2. Note that it's also inverting, so both VC1 and VC1 rise and fall together with a common mode input as you'd expect with a current mirror.



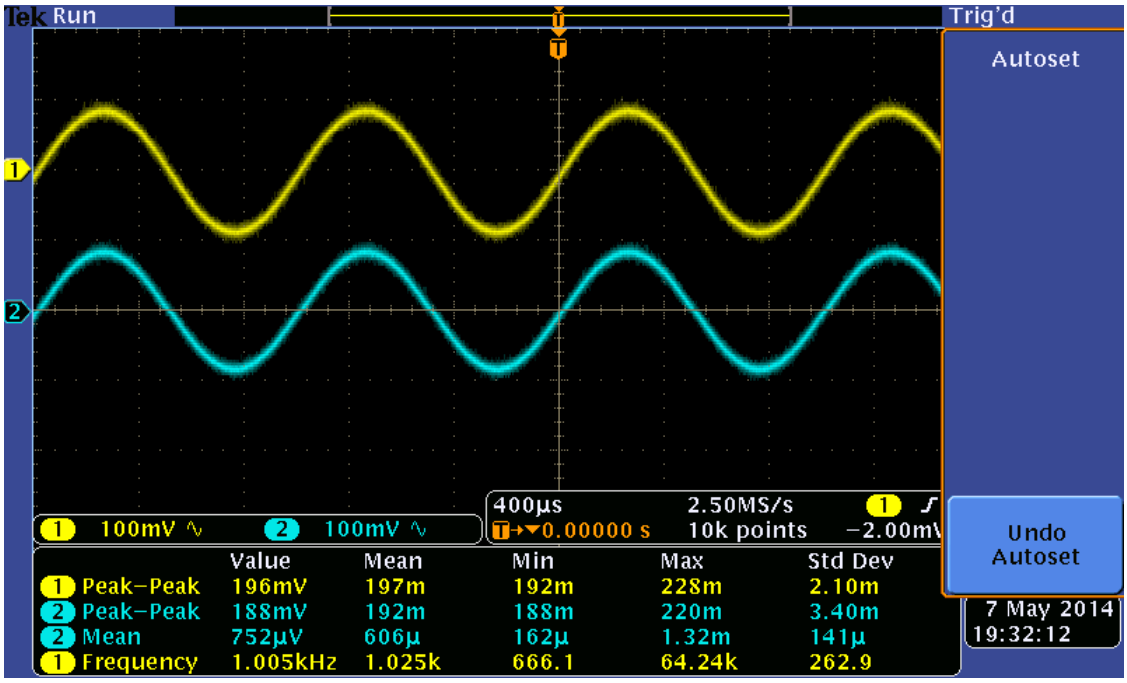
2. Av1 = VC1 / Vin = -1.61 / 2.99 = -0.54 (inverting).
   Av2 = VC2 / Vin = -1.19 / 2.99 = -0.40 (inverting).

3. The 3 db point would be where Av = 0.7071 * 0.54 = 0.38. Here I've measured Av1 = 1.13 / 2.99 = 0.38 at 2.6 MHz.

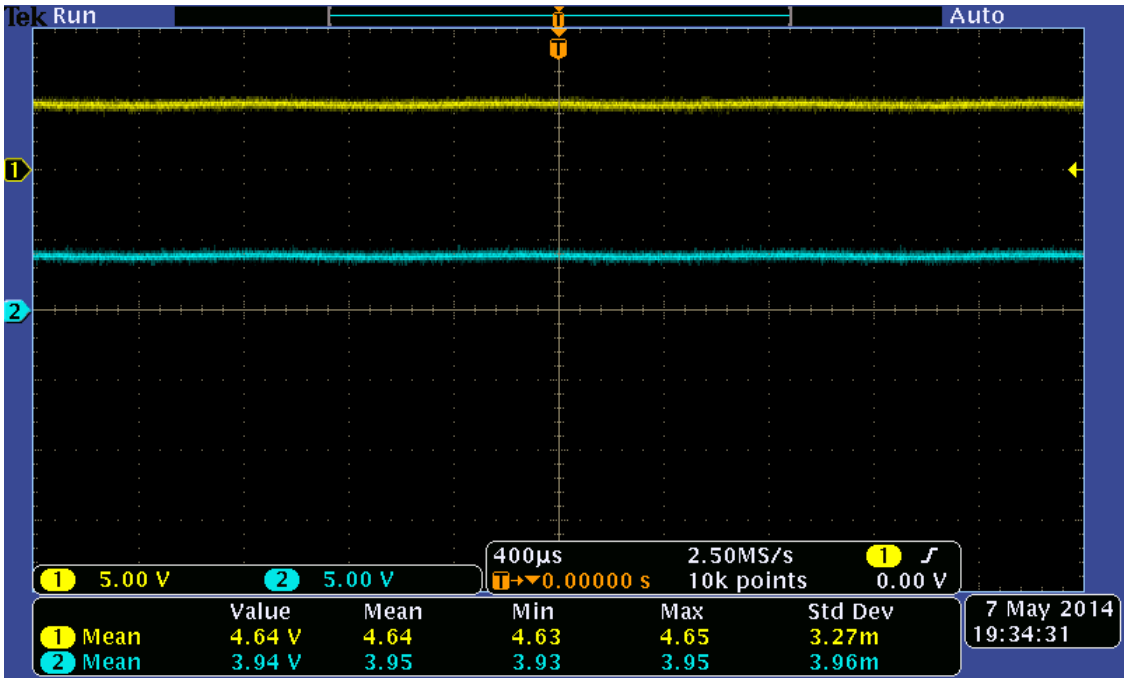


4. You were next asked to take measurements with Vin = 200 mVpp, 1.0 KHz sine wave, DC offset = +4.9 V. Again, you only needed to measure either VC1 or VC2, not both.

   Here's the AC-coupled measurement. Av (small signal) = 192 / 197 = 0.97. The output is not inverted. (This is not a perfect screenshot. It happens to us all.)



   Here's the DC-coupled measurement. The DC offset in the output is about 3.95 V. Av (DC) = 3.94 / 4.64 = 0.85.



7.4 Analysis

1. Calculate the common-mode rejection ration (CMRR) as both a ratio and in db.

   CMRR = Av (differential) / Av (common) = 37.3 / 0.54 = 69

   CMRR (db) = 20 log10(CMRR) = 37 db

2. Explain why common mode gain ≈ 0.5 and inverting when no DC offset is applied.

   Each side of the differential pair is a common emitter amplifier. The gain of a common emitter amplifier is approximately RC / RE. But because we have an equal current through RE from the other leg of the differential pair, the IR drop across RE will be twice what it would be if RE wasn't shared. That effectively doubles RE, resulting in a gain RC/(2*RE) = 0.5.

3. Explain why common mode gain jumps to about 1.0 and becomes non-inverting when a DC offset is applied.

   When VB is high enough, both the BC and the BE junctions are forward-biased, putting the transistor into saturation.

4. Suggest a way to increase CMRR.

   Substitute one leg of a current mirror for RE.